What is claimed is:

1. A write operation for a non-volatile memory, comprising:

(a) applying a first programming voltage to a word line that is connected to multiple selected memory cells that are being simultaneously programmed to respective target threshold voltages that represent respective values being written;

(b) applying a second programming voltage to a set of column lines that are connected to the selected memory cells, wherein application of the first programming voltage and the second programming voltage change threshold voltages of the selected memory cells; and

(c) determining which of the selected memory cells have reached the respective target threshold voltages that represent the respective values;

(d) removing from the set of column lines any column lines connected to the selected memory cells determined to have reached the respective target threshold voltages;

(e) changing the first programming voltage; and

(f) repeating steps (a) to (e) until the set of column lines is empty, wherein for a series of repetitions of step (e) an amount of change in the first programming voltage differs from amounts of change in preceding executions of step (e).

2. The operation of claim 1, wherein the amount of change in the first programming voltage is less than the amounts of change in preceding repetitions of step (e).

3. The operation of claim 1, further comprising changing the second programming voltage each time the first programming voltage changes.

4. The operation of claim 1, wherein at least one of the repetitions of step (a) has a duration that is less than a duration of a preceding execution of step (a).

5. The operation of claim 1, wherein each repetition of step (a) has a duration equal to the duration of other repetitions of step (a).

6. The operation of claim 1, wherein the repetitions of step (a) are partitioned into a first set of programming cycles each of which has a first duration and a second set of programming cycles each of which has a second duration.

7. The operation of claim 6, wherein each of the programming cycles in the first set is before all of the programming cycles in the second set.

8. The operation of claim 7, wherein the first set contains a single programming cycle.

9. The operation of claim 8, wherein the first duration is sufficiently long so that by an end of the programming cycle in the first set a rate of programming a typical memory cell becomes small relative to a ratio of a difference between two of the target threshold voltage levels and the second duration.

10. The operation of claim 1, wherein each of the values being written comprises multiple bits.

11. A write operation for a non-volatile memory, comprising:

(a) applying a first programming voltage to a word line that is connected to multiple selected memory cells that are being simultaneously programmed to respective target threshold voltages that represent respective values being written;

(b) applying a second programming voltage to a set of column lines that are connected to the selected memory cells, wherein application of the first programming voltage and the second programming voltage change threshold voltages of the selected memory cells; and

(c) determining which of the selected memory cells have reached the respective target threshold voltages that represent the respective values;

(d) removing from the set of column lines any column lines connected to the selected memory cells determined to have reached the respective target threshold voltages; and

(e) repeating steps (a) to (d) until the set of column lines is empty, wherein for a series of repetitions of step (a) a duration of application of the first programming voltage differs from durations of preceding executions of step (a).

12. The write operation of claim 11, wherein each duration of a repetition of step (a) is less than the duration of a preceding execution of step (a).

13. The write operation of claim 11, wherein each of the values being written comprises multiple bits.

14. The write operation of claim 11, wherein a first N of the repetitions of step (a) that occurs first during the write operation have a first duration and all other repetitions of step (a) have a second duration.

15. The operation of claim 14, wherein N is equal to 1.

16. The operation of claim 15, wherein the first duration is sufficiently long so that by an end of the first programming cycle, a rate of programming of a typical memory cell becomes small relative to a ratio of a difference between two of the target threshold voltage levels and the second duration.

17. A write operation for a non-volatile memory, comprising applying a write signal to a word line that is connected to multiple selected memory cells that are being simultaneously programmed, wherein the selected memory cells are being programmed to respective target threshold voltages that represent respective multi-bit data values being written, and the write signal includes:

a plurality of programming cycles during which programming voltages applied to the selected memory cells change threshold voltages of the selected memory cells; and

a plurality of verify cycles during which sensing operations determine whether the

selected memory cells have reached the respective target threshold voltages, wherein

the programming cycles have shorter duration at an end of a first interval than at a start of the first interval; increase in duration immediately after the first interval, and for a second interval that follows the first interval have shorter duration at an end of the second interval than at a start of the second interval.

18. The write operation of claim 17, wherein the programming cycles are such that programming of a typical memory cell reaches a first of the target threshold voltages near the end of the first interval and reaches a second of the target threshold voltages near the end of the second interval.

19. The write operation of claim 17, further comprising:

biasing drains of the selected memory cells to a first level during the first interval, wherein the programming cycles are such that programming of a typical memory cell having a drain biased at the first level reaches a first of the target threshold voltages near the end of the first interval; and

biasing the drains of the selected memory cells that are being programmed to a second of the target threshold voltage to a second level during the second interval, wherein the second level differs from the first level, and programming of a typical memory cell having a drain biased at the second level reaches the second of the target threshold voltages near the end of the second interval.

20. The write operation of claim 17, further comprising:

biasing sources of the selected memory cells to a first level during the first interval, wherein the programming cycles are such that programming of a typical memory cell having a source biased at the first level reaches a first of the target threshold voltages near the end of the first interval; and

biasing the sources of the selected memory cells that are being programmed to a second of the target threshold voltage to a second level during the second interval, wherein the second

level differs from the first level and programming of a typical memory cell having a source biased at the second level reaches the second of the target threshold voltages near the end of the second interval.

21. A write operation for a non-volatile memory, comprising:

(a) starting an interval for programming that includes:

(b) applying first programming pulses to a word line that is connected to multiple selected memory cells that are being simultaneously programmed to respective target threshold voltages that represent respective values being written;

(b) applying second programming pulses to a set of column lines that are connected to the selected memory cells, wherein application of the first programming pulses and the second programming pulses change threshold voltages of the selected memory cells; and

(c) determining which of the selected memory cells have reached a target threshold voltage that corresponds to the interval;

(d) removing from the set of column lines any column lines connected to the selected memory cells that was determined to have reached the target threshold voltage corresponding to the interval;

(e) repeating steps (b) to (d) until the set of column lines is empty; and

(f) repeating steps (a) to (e) until the selected memory cells have reached the respective target threshold voltages.

22. The write operation of claim 21, wherein during each of the intervals, at least one of the first programming pulse applied to the word line at the start of the interval has an initial voltage level depends on the target threshold voltage corresponding to the interval.

23. The write operation of claim 22, wherein during each of the intervals interval, at least one of the first programming pulses applied to the word line near an end of the interval has a voltage level that is greater than the initial voltage.

24. The write operation of claim 22, wherein for each repetition of steps (a) to (e), the initial voltage at the start of the interval is greater than the initial voltage at the start of a previous interval.

25. The write operation of claim 24, wherein for at least one of the intervals, at least one of the first programming pulses applied to the word line near an end of the interval has a voltage level that is greater than the initial voltage for a following one of the intervals.

26. The write operation of claim 21, wherein during each of the intervals interval, at least one of the first programming pulses applied to the word line near an end of the interval is shorter than at least one of the first programming pulses applied to the word line near a beginning of the interval.

27. The write operation of claim 26, wherein for each of the intervals interval, each of the first programming pulses has either a first duration or a second duration.

28. The write operation of claim 21, wherein during each interval the second programming pulse have a voltage level depends on the target threshold voltage corresponding to the interval.

29. The write operation of claim 21, wherein each repetition of step (a) is in response to and immediately follows determining that the set of column lines is empty.

30. The write operation of claim 21, wherein each of the intervals has a duration that depends on an amount of time before the set of column lines becomes empty